AMENDMENTS TO THE SPECIFICATION:

Page 2, the second full paragraph, continuing to page 3, was amended as follows:

Thus, currently, the most appropriate method to implement low K materials between tightly spaced interconnect lines is utilizing air gaps between interconnect lines. The air gap formation permits the utilization of air as an intra-level dielectric material, which has the relative dielectric constant of 1.0, which is much lower than the relative dielectric constants of other conventional materials. However, as shown in the drawing of figure 1, the conventional process for forming air gaps in the substrate, having interconnect lines formed thereon, includes depositing an inter-metal dielectric layer 2 over the substrate 1 to form air gaps 3, 4 between the interconnect lines. Due to the fact that the spacing between the interconnect lines is varied, the spacing is larger, and the air gap is formed higher from the substrate 1, such as air gap 4. When the subsequently proceeding CMP process is performed on ~~for~~ the inter-metal dielectric layer 2, the higher air gap 4 is ~~open~~ opened up by the CMP process, then an acid, such as ~~acid,~~ Alumina will enter into the inter-metal dielectric layer 2 to result in ~~this layer works fail~~ the failure of this layer. Moreover, the air gap is formed faster near the lateral wall of the bottom of the interconnect lines, and the hole of the air gap is tapered from the bottom to the top of the air gap. Thus, the low K effect of the conventional air gap is not ~~well~~ good.

Page 3, the second full paragraph was amended as follows:

The primary object of the invention is to provide a method for reducing capacitance between interconnect lines, ~~which~~ where forming a pad oxide layer on each of the metal

lines to form an interconnect line, thereby ~~increase~~ increases the intra-metal aspect ratio to facilitate air gap formation in the spacing between adjacent interconnect lines.

Page 3, the third full paragraph, continuing to page 4, was amended as follows:

Another object of the invention is to provide a method for reducing capacitance between interconnect lines, which forms a more ideal air gap in the spacing between adjacent metal lines, the upper and lower ends of the air gap respectively exceeding the top and bottom ends of the adjacent metal lines, and the distance from the portion of the air gap between the top and bottom ends of the metal line to the sidewall of the metal line is more consistent and smaller, so as to minimize the difference of the low K effect of the portion of the air gap and ~~give~~ provide a better low K effect.

Page 4, the first full paragraph was amended as follows:

A further object of the invention is to provide a method for reducing capacitance between interconnect lines, which forms a pad oxide layer on each of metal lines to form an interconnect line, so that an air gap is formed in the spacing between the adjacent interconnect lines under the top end of the pad oxide layer. Therefore, the air gap is not damaged while proceeding with the subsequent CMP process.

Page 4, the second full paragraph was amended as follows:

A still further object of the present invention is to provide an interconnect structure for reducing capacitance between interconnect lines, which is characterized in that each of the air gaps in the spacings of adjacent interconnect lines each of which ~~comprising~~

includes a lower metal line and ~~a~~ an upper pad oxide layer is formed below the top end of the pad oxide layer with more consistent and smaller spacing between the air gap and the sidewall of the metal line.

Page 6, the first paragraph was amended as follows:

Referring to FIG. 2, the present invention includes firstly providing a substrate 5, having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon (not shown in the figure); depositing a metal layer 6 over the substrate 5, the metal layer 6 ~~can be~~ including an aluminum layer deposited by a DC sputtering deposition method, about 3000-10000 ~~angstronm~~ angstrom thickness, the metal layer 6 also ~~can be~~ including being formed by metals selected from the group consisting of Cu, Ta, Au, Pb, Si, W and Sn; then depositing a pad oxide layer 7 over the metal layer 6 with a thickness between about 2000 ~~angstronm~~ angstrom and about 5000 ~~angstronm~~ angstrom, the pad oxide layer 7 ~~can be~~ including a SiO_2 layer, deposited by an atmospheric pressure CVD method, utilizing SiH_4 as a reaction gas, under the pressure of 0.5~1 torr, at a temperature of 400~500°C. Alternatively, the pad oxide layer 7 can be deposited by a plasma enhanced CVD method, utilizing SiH_4 as a reaction gas, under the pressure of 1~10 torr, at a temperature of 300~400°C. Otherwise, it is deposited by a plasma enhanced CVD method, utilizing TEOS/O3 as a reaction gas.

Page 6, the second paragraph was amended as follows:

Referring to FIG. 3, subsequently, patterning and etching the pad oxide layer 7 and metal layer 6 by the conventional lithography and etching technique to constitute adjacent

interconnect lines 8, is performed.